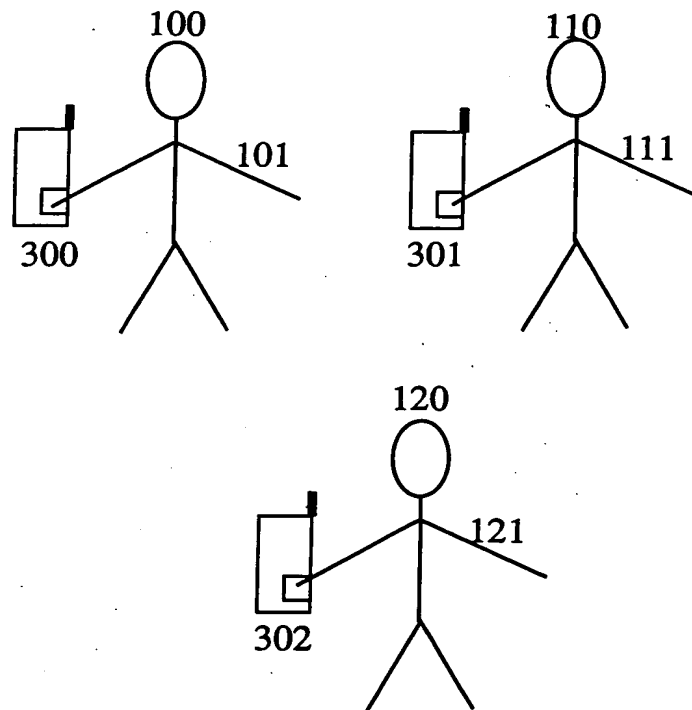


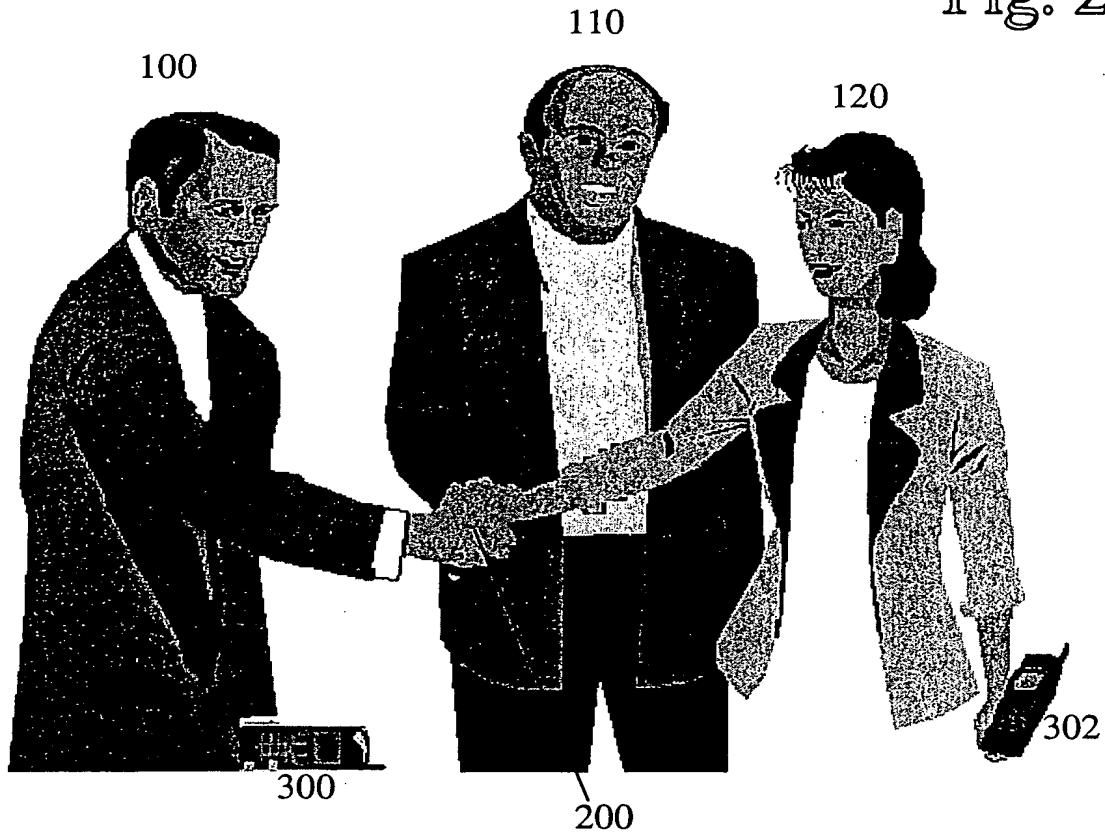
Fig. 1



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Fig. 2



10027501.01.502

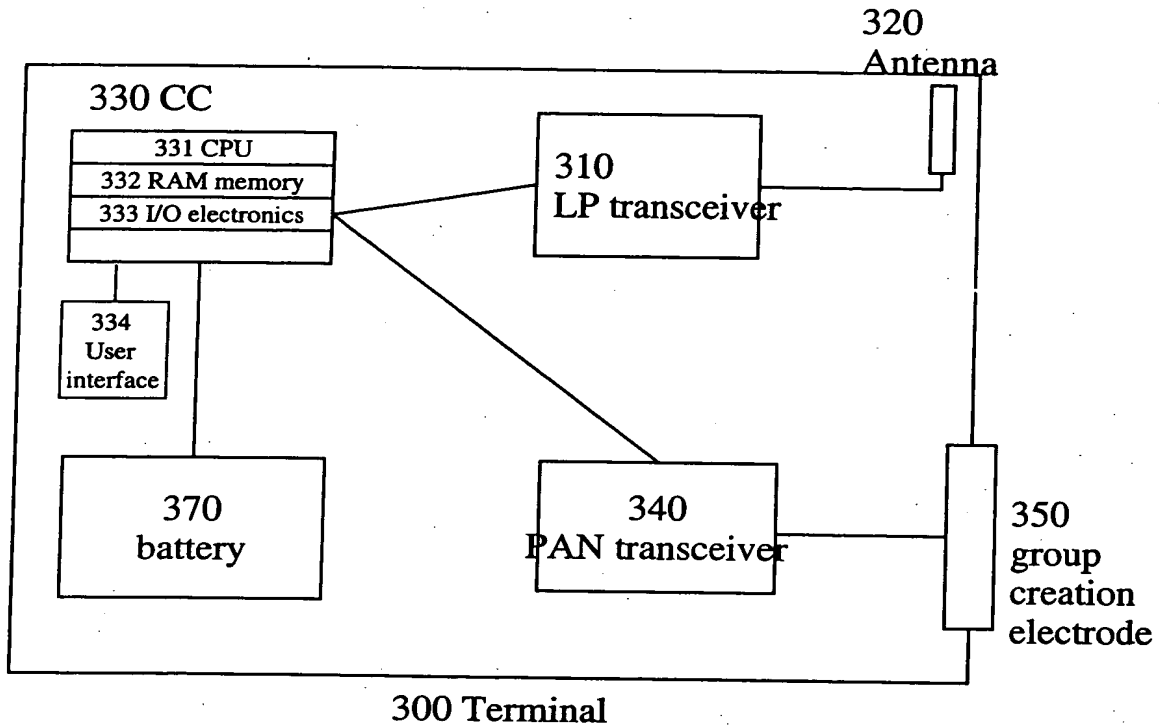


Fig. 3

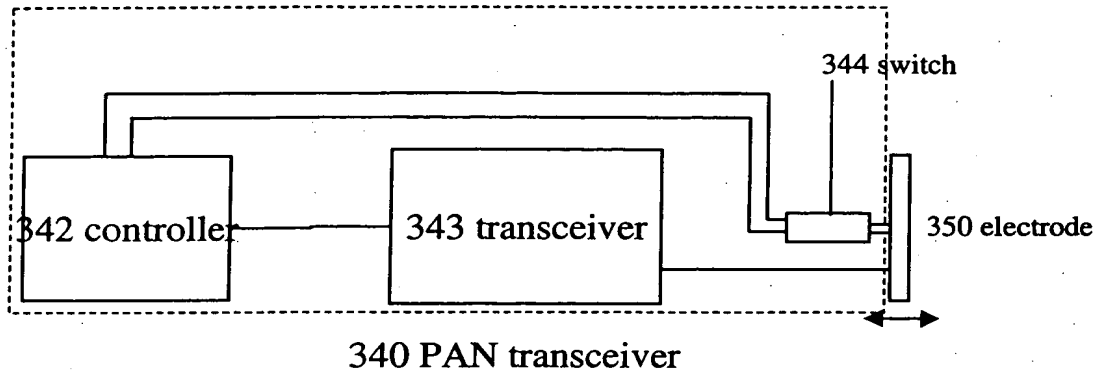


Fig. 4A

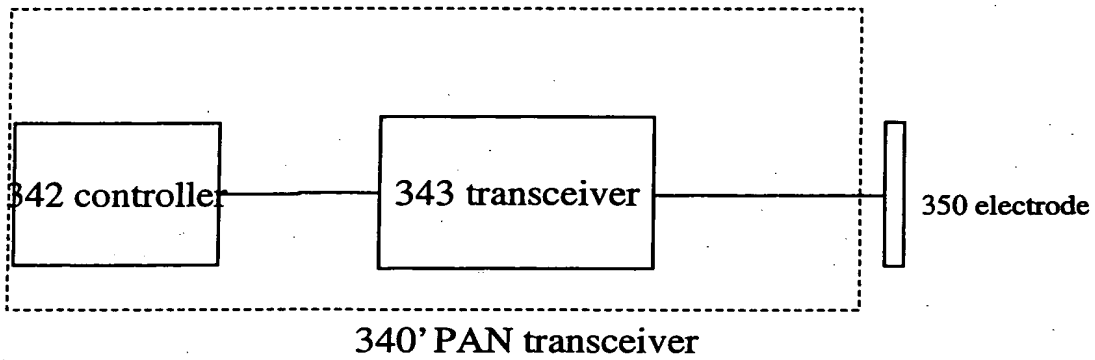


Fig. 4B

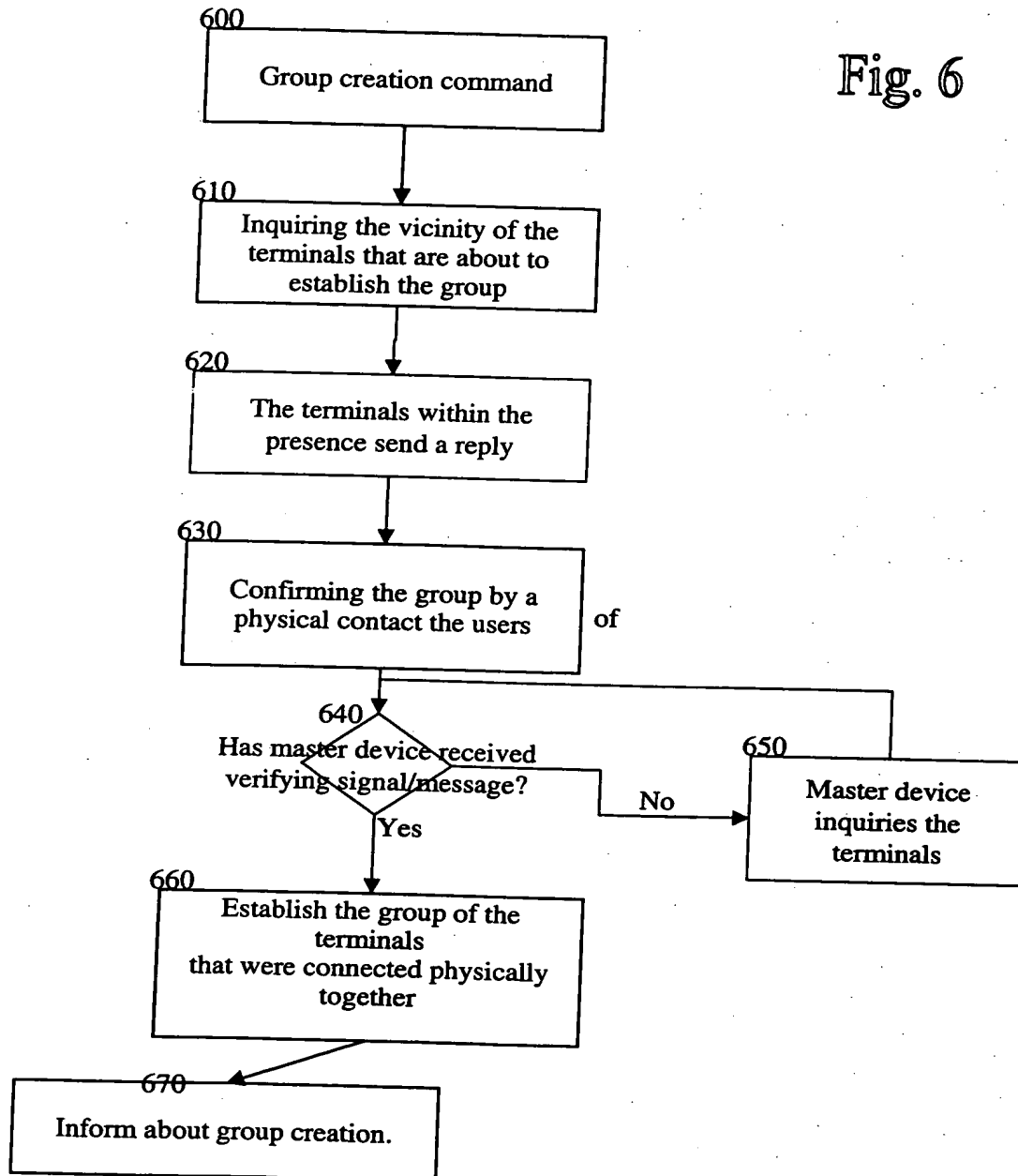
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501	502	503	
BD_ADDR	Clock Offset	Class of Device	

Fig. 5

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Fig. 6



10027501.01.1.502

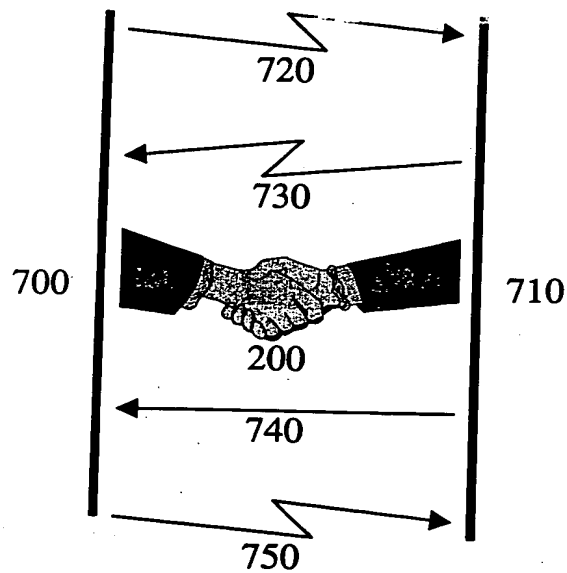


Fig. 7

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Fig. 8

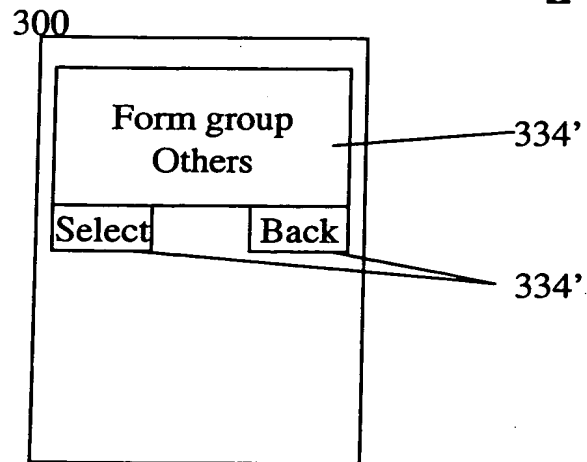
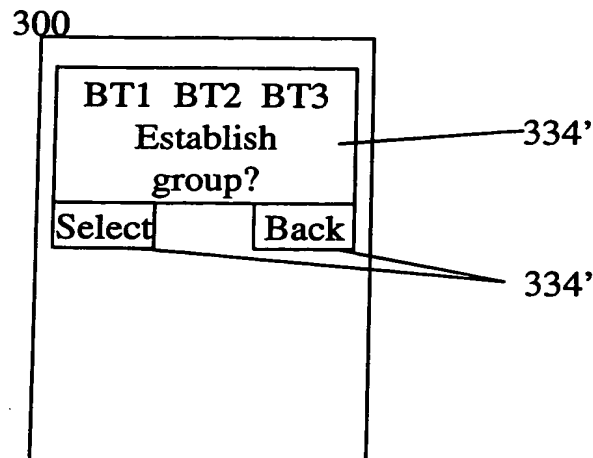


Fig. 9



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